

**AMENDMENT TO THE CLAIMS**

1 – 6 (Previously canceled)

7. (Original) A method for improving the routing of signals through an array macro embedded in a semiconductor chip wherein the macro comprises a plurality of slices, each having different porosities depending on the number of channels extending therethrough, the method comprising the steps of:

- (a) developing a chip floor plan including early timing allocation and proposed array placement;
- (b) flagging critical logical wiring nets and overlaying the floor plan with the nets;
- (c) making an initial selection of slices for the macro based upon the number of channels required at each location within the macro; and
- (d) assembling the macro with the placement of slices to provide porosities based upon the channel requirements.

8. (Previously presented) The method according to claim 7 wherein the slices divide a plurality of functional blocks wherein blocks with the same functionality have the same height and width.

9. (Original) The method according to claim 7 wherein the step of chip floor planning includes establishing a base level of porosity in the chip.

10. (Original) The method according to claim 7 wherein the array comprises a field programmable gate array.

11. (Original) The method according to claim 7 including the further step of changing slices after floor planning to make further adjustments in porosity.

12. (Original) The method according to claim 11 wherein the changes occur during the execution phase of chip design prior to chip construction.

13. (Currently amended) A macro for use ~~in~~ as a field programmable gate array integrated circuit embedded in a semiconductor chip, said macro containing a plurality of pre-wired slices, each of which has a unique porosity factor representing the number of contiguous wiring channels within the slice, the slices positioned at locations within the chip wherein the number of wiring channels in each slice corresponds to the number of circuit lines in the chip macro available for chip-level wiring between other integrated circuits on said semiconductor chip, said wires passing entirely through the said macro at each slice location within the macro.

14-16 (Previously canceled)

17. (Currently amended) The macro according to claim 13 wherein the pre-wired slices have identical masses, and the size of each slice corresponds to the degree of porosity of the slice.

18-23 (Canceled)